Am25L02/25L03/25L04

Low-Power, Eight-Bit/Twelve-Bit Successive Approximation Registers

Distinctive Characteristics

- Contains all the storage and control for successive approximation A-to-D converters.
- Can be operated in START-STOP or continuous conversion mode.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Can be used as serial-to-parallel converter or ring counters.

FUNCTIONAL DESCRIPTION

The Am25L02, Am25L03 and Am25L04 are 8-bit and 12-bit TTL Successive Approximation Registers. The registers contain all the digital control and storage necessary for successive approximation analog-to-digital conversion. They can also be used in digital systems as the control and storage element in recursive digital routines.

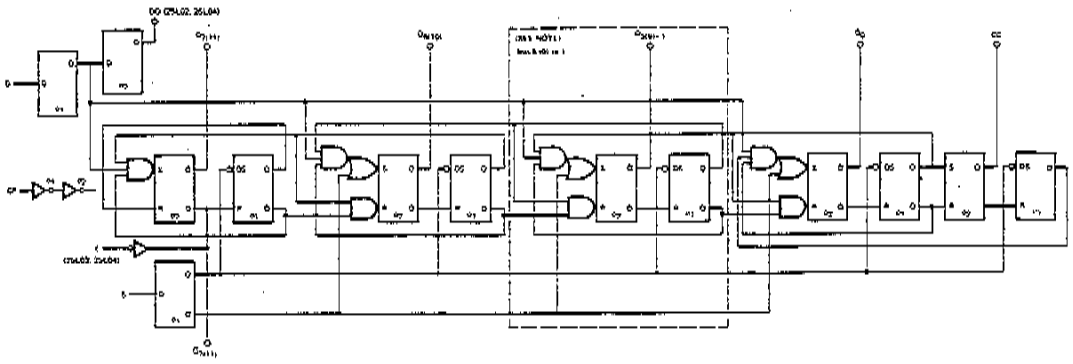
The registers consist of a set of master latches that act as the control elements in the device and change state when the input clock is LOW, and a set of slave latches that hold the register data and change on the input clock LOW-to-HIGH transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the Am25L02 and Am25L04 when the clock goes from LOW-to-HIGH. There are no restrictions on the data input; it can change state at any time except during the set-up time just prior to the clock transition. At the same time that data enters the register bit the next less significant bit is set to a LOW ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal LOW during the clock LOW-to-HIGH transition. The register synchronously resets to the state $Q_7(11)$ LOW, (Note 2) and all the remaining register outputs HIGH. The $\overline{CC}$ (Conversion Complete) signal is also set HIGH at this time. The $\overline{S}$ signal should not be brought back HIGH until after the clock LOW-to-HIGH transition in order to guarantee correct resetting.

After the clock has gone HIGH resetting the register, the $\overline{S}$ signal is removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the $Q_7(11)$ register bit and the $Q_6(10)$ register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH transition data enters the $Q_6(10)$ register bit and $Q_5(9)$ is set to a LOW. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q_0, the $\overline{CC}$ signal goes LOW, and the register is inhibited from further change until reset by a Start signal.

In order to allow complementary conversion the complementary output of the most significant register bit is made available. An active LOW enable input, $\overline{E}$, on the Am25L03 and Am25L04 allows devices to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs together and connecting the $\overline{CC}$ output of one device to the $\overline{E}$ input of the next less significant device. When the Start signal resets the register, the $\overline{E}$ signal goes HIGH, forcing the $Q_7(11)$ bit HIGH and inhibiting the device from accepting data until the previous device is full and its $\overline{CC}$ goes LOW. If only one device is used the $\overline{E}$ input should be held at a LOW logic level (Ground). For continuous conversion the $\overline{CC}$ output is connected to the $\overline{S}$ input so that the device automatically restarts at the end of a conversion. If all the bits are not required, the register may be truncated and conversion time saved by using a register output going LOW rather than the $\overline{CC}$ signal to indicate the end of conversion.

LOGIC DIAGRAMS



Notes: 1. Cell logic is repeated for register stages. Q_5 to Q_1 Am25L02/3, Q_9 to Q_1 Am25L04.
2. Numbers in parentheses are for Am25L04.

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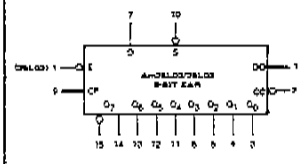
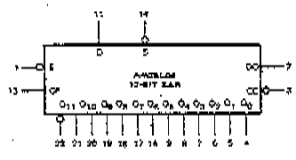
LOGIC SYMBOLS



LIC-235

V_{CC} = Pin 16
GND = Pin 8



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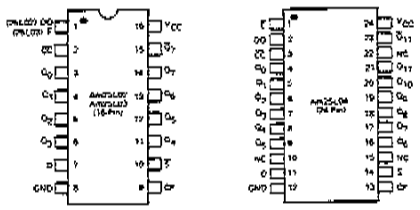
V_{CC} = Pin 24
GND = Pin 12
NC = Pins 10, 15 22

CONNECTION DIAGRAMS

Top Views



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Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25L02XC, Am25L03XC, Am25L04XC: T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%
Am25L02XM, Am25L03XM, Am25L04XM: T_A = −55°C to +125°C, V_{CC} = 5.0V ±10%

Parameters	Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.4mA, V_{IN} = V_{IH} or V_{IL}			2.4	3.6		Volts
V_{OL}	Output LOW Voltage (Note 2)	V_{CC} = MIN., I_{OL} = 4.92mA, V_{IN} = V_{IH} or V_{IL}				0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.7	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.3V		CP, D, $\overline{S}$		−0.25	−0.4	mA
				$\overline{E}$		−0.4	−0.6	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V		CP, D		2.0	20	µA
				$\overline{E}$, $\overline{S}$		4.0	40	
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V			4.0	15	35	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	Am25L02	XM		25	33	mA
				XC		25	35	
			Am25L03	XM		22	31	mA
				XC		22	33	
			Am25L04	XM		30	42	mA
				XC		30	45	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. V_{OL}(MAX) = 0.3V with total device fanout of less than 90 Low Power TTL Unit Loads (36mA), otherwise, V_{OL}(MAX) = 0.35V.

Switching Characteristics (T_A = 25°C, V_{CC} = 5.0V, C_L = 15pF)

Parameters	Description		Min.	Typ.	Max.	Units
t_{pd+}	Turn Off Delay CP to Output HIGH (except Q_{11}, $\overline{Q}_{11}$)		20	75	110	ns
t_{pd+}	Turn Off Delay CP to Q_{11} or $\overline{Q}_{11}$ HIGH		30	100	140	ns
t_{pd-}	Turn On Delay CP to Output LOW		20	75	100	ns
t_s(D)	Set-up Time Data Input		−15	8.0	20	ns
t_s(S)	Set-up Time Start Input		0	20	25	ns
t_{pd+}(E)	Turn Off Delay $\overline{E}$ to Q_7(11) HIGH	(Am25L03/Am25L04)		50	75	ns
t_{pd-}(E)	Turn On Delay $\overline{E}$ to Q_7(11) LOW	CP = H, S = L		60	75	ns
t_{pwL}(CP)	Minimum LOW Clock Pulse Width			100	150	ns
t_{pwH}(CP)	Minimum HIGH Clock Pulse Width			70	100	ns
$f_{max.}$	Maximum Clock Frequency		3.5	5.0		MHz

Am25L02/3 TRUTH TABLE

Time	Inputs			Outputs									
t_n	D	$\overline{S}$	$\overline{E}$	D_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D_7	H	L	X	L	H	H	H	H	H	H	H	H
2	D_6	H	L	D_7	D_7	L	H	H	H	H	H	H	H
3	D_5	H	L	D_6	D_7	D_6	L	H	H	H	H	H	H
4	D_4	H	L	D_5	D_7	D_6	D_5	L	H	H	H	H	H
5	D_3	H	L	D_4	D_7	D_6	D_5	D_4	L	H	H	H	H
6	D_2	H	L	D_3	D_7	D_6	D_5	D_4	D_3	L	H	H	H
7	D_1	H	L	D_2	D_7	D_6	D_5	D_4	D_3	D_2	L	H	H
8	D_0	H	L	D_1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	L	H
9	X	H	L	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
10	X	X	L	X	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

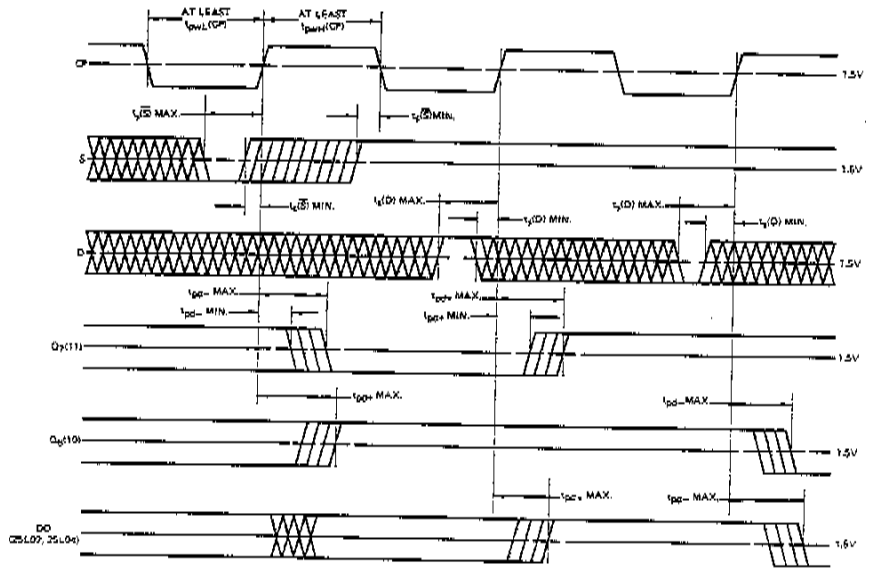
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change

Note: Truth Table for Am25L04 is extended to include 12 outputs.

USER NOTES FOR A/D CONVERSION

1. The register can be used with either current switches that require a low voltage level to turn the switch on, or current switches that require a high voltage level to turn the current switch on. If current switches are used which turn on with a low logic level the resulting digital output from the register is active LOW. That is, a logic "1" is represented as a low voltage level. If current switches are used that turn on with a high logic level then the digital output is active HIGH; a logic "1" is represented as a high voltage level.
2. For a maximum digital error of ±½LSB the comparator must be biased. If current switches that require a low voltage level to turn on are used, the comparator should be biased +½LSB and if the current switches require a high logic level to turn on then the comparator must be biased −½LSB.
3. The register, by suitable selection of resistor ladder network, can be used to perform either binary or BCD conversion.
4. The register can be used to perform 2's complement conversion by offsetting the comparator ½ full range +½ LSB and using the complement of the MSB Q_7 (11) as the sign bit.
5. If the register is truncated and operated in the continuous conversion mode a lock-up condition may occur on power-on. This situation can be overcome by making the START input the OR function of $\overline{CC}$ and the appropriate register output.

SWITCHING TIME WAVEFORMS



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN

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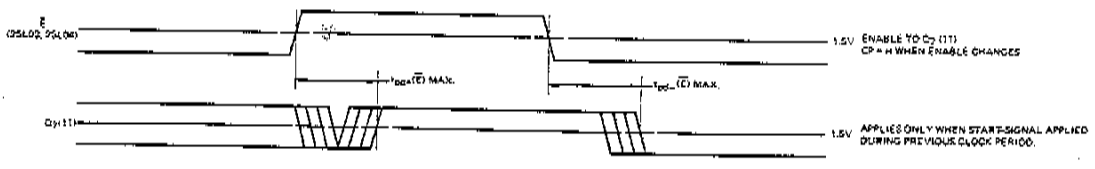

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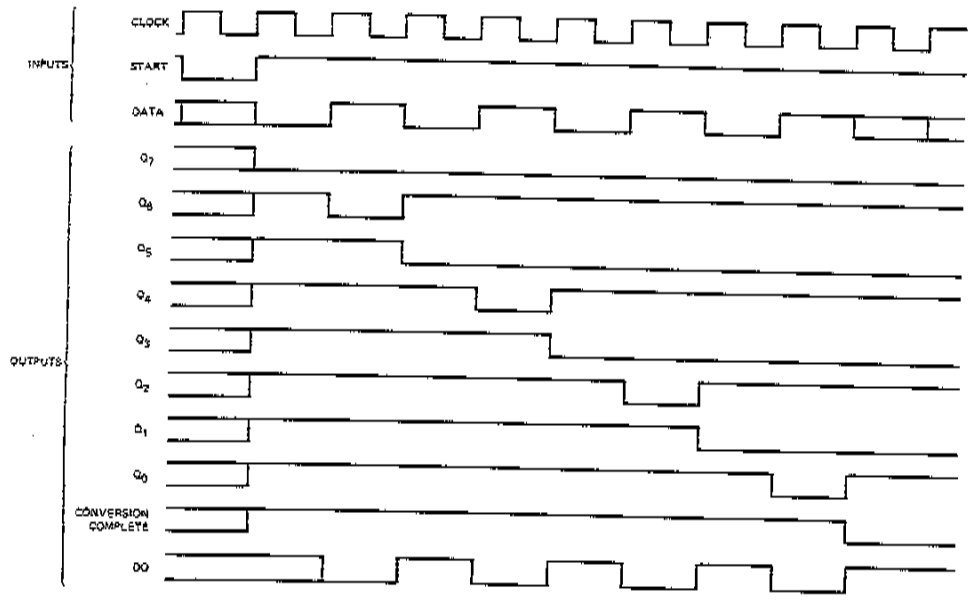
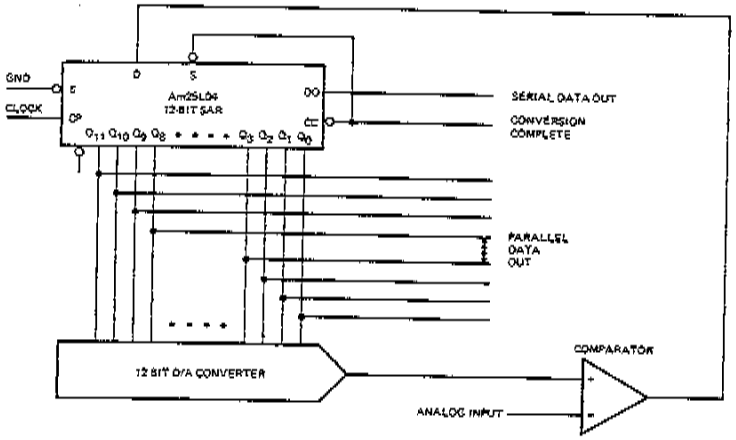
Am25L02/3 TIMING CHART



LIC-241

Am25L02/3/4 APPLICATION
Continuous Conversion Analog-to-Digital Converter



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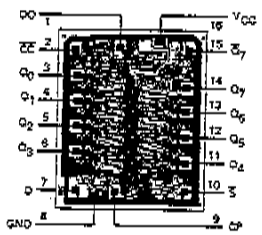
This shows how the Am25L02/3/4 registers are used with a Digital-to-Analog converter and a comparator to form a very high-speed continuous conversion Analog-to-Digital converter. Conversion time is limited mainly by the speed of the D/A converter and comparator with typical conversion rates of 300,000 conversions per second. The comparator can be the Am111 precision comparator, or Am106 high-speed comparator.

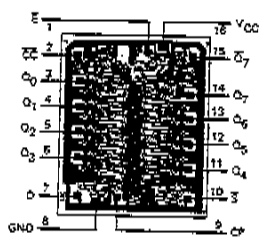
Metallization and Pad Layout

Am25L02



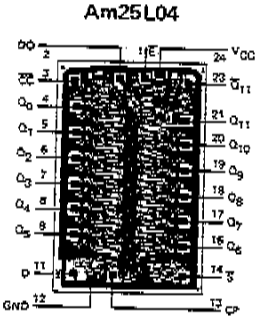
DIE SIZE 0.087" X 0.105"

Am25L03



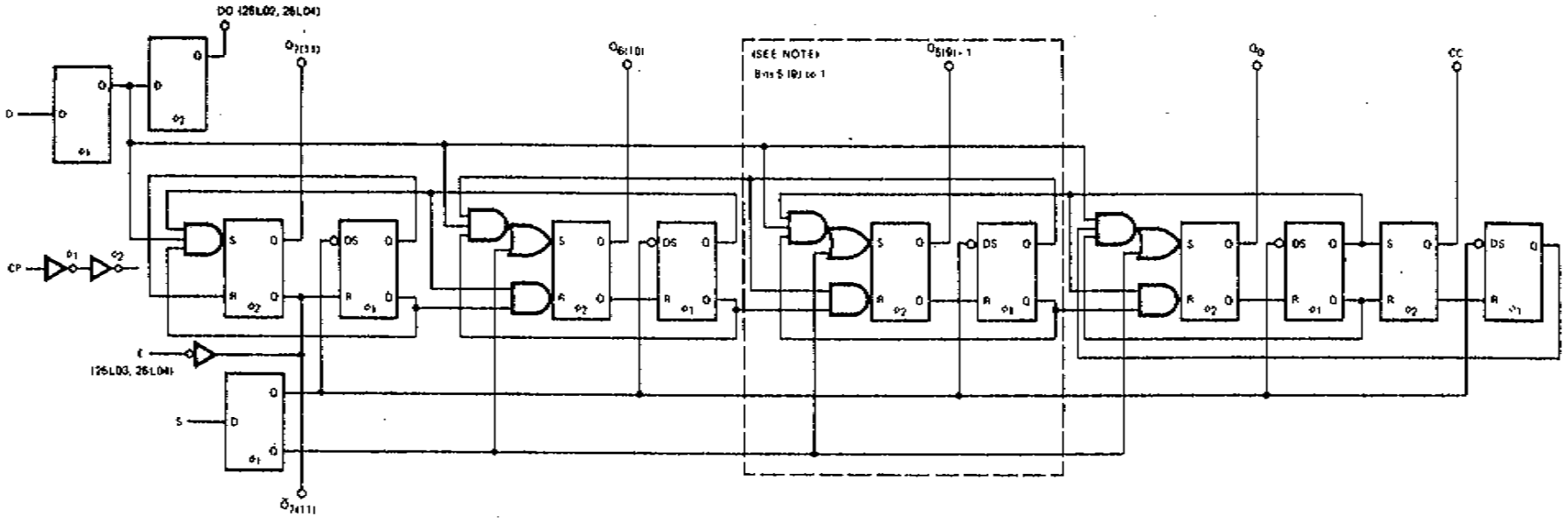
DIE SIZE 0.087" X 0.105"

Am25L04



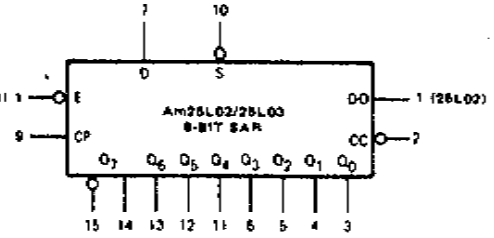
DIE SIZE 0.087" X 0.135"

LOGIC DIAGRAMS



Notes: 1. Cell logic is repeated for register stages. Q_5 to Q_1 Am25L02/3, Q_9 to Q_1 Am25L04.
2. Numbers in parentheses are for Am25L04.

LOGIC SYMBOLS



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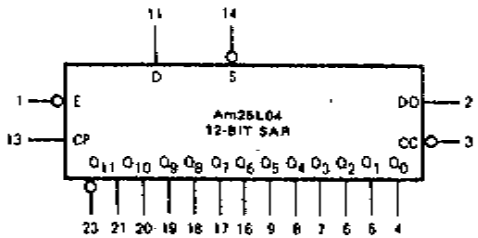
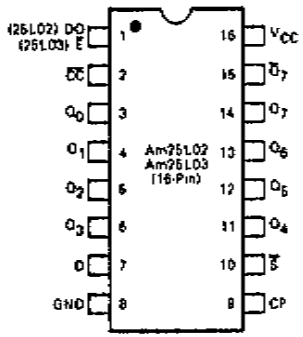
V_{CC} = Pin 16
GND = Pin 8

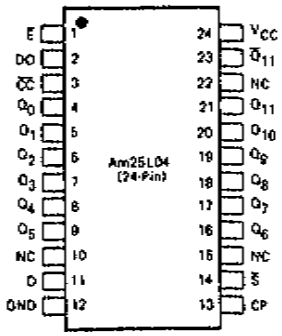


LIC-236

V_{CC} = Pin 24
GND = Pin 12
NC = Pins 10, 15 22

CONNECTION DIAGRAMS
Top Views





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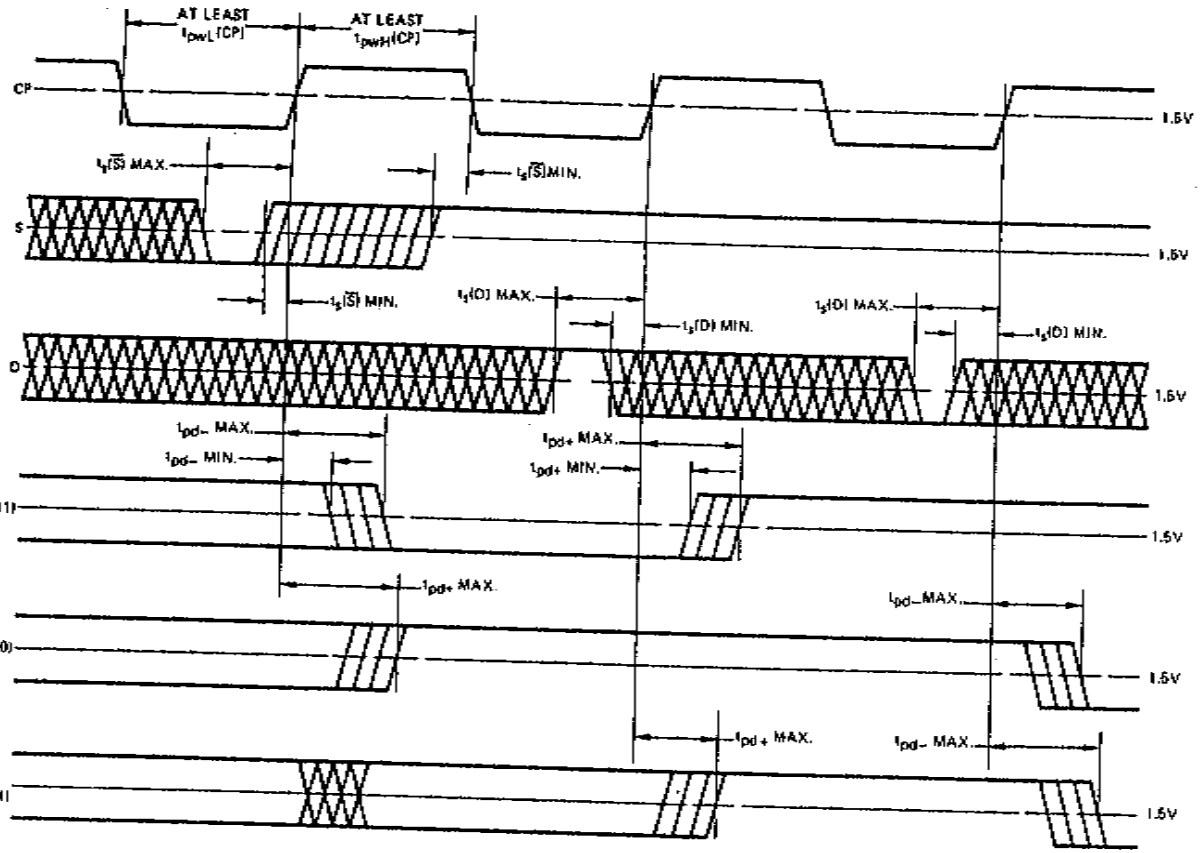
Note: Pin 1 is marked for orientation.

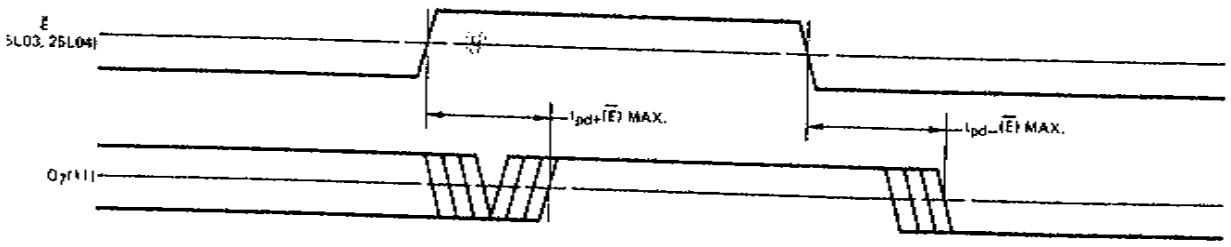
SWITCHING TIME WAVEFORMS



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN

LIC-239



ENABLE TO Q_7 (11)
CP = H WHEN ENABLE CHANGES

APPLIES ONLY WHEN START-SIGNAL APPLIED DURING PREVIOUS CLOCK PERIOD.

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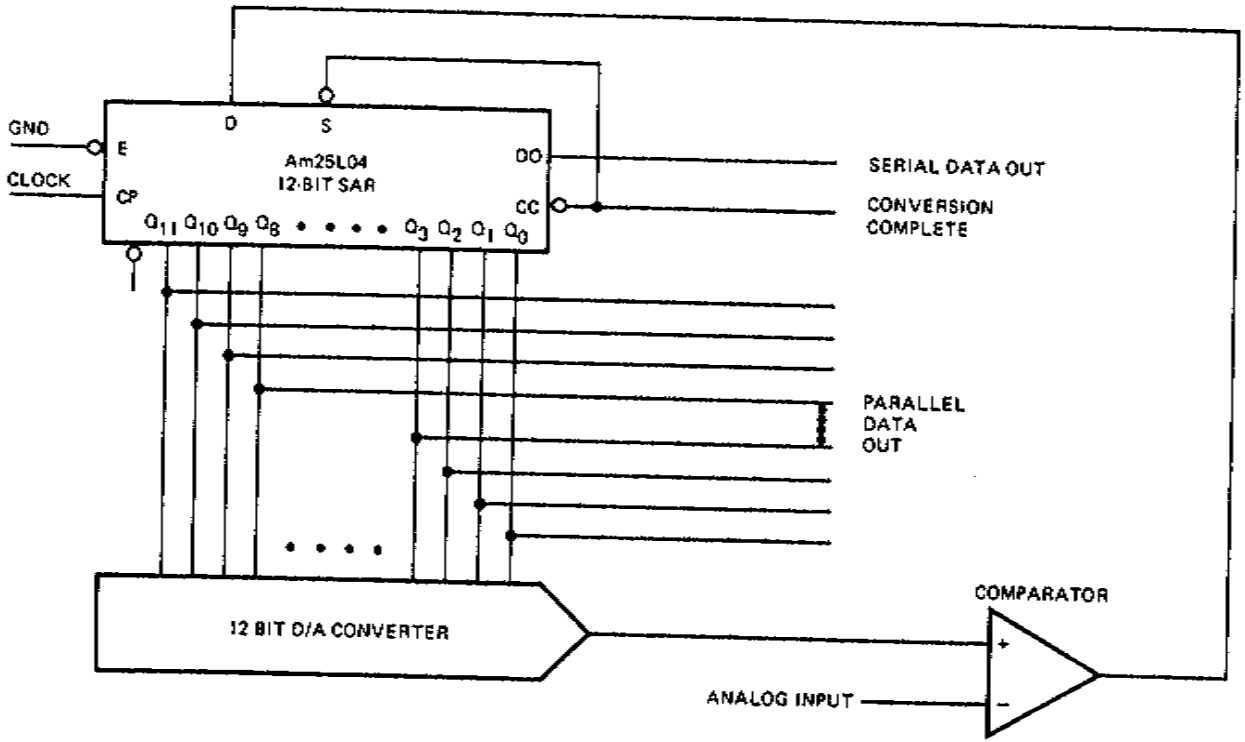
Am25L02/3/4 APPLICATION
Continuous Conversion Analog-to-Digital Converter

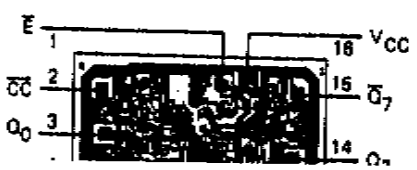


This shows how the Am25L02/3/4 registers are used with a Digital-to-Analog converter and a comparator to form a ver continuous conversion Analog-to-Digital converter. Conversion time is limited mainly by the speed of the D/A converter and with typical conversion rates of 300,000 conversions per second. The comparator can be the Am111 precision comparato high-speed comparator.

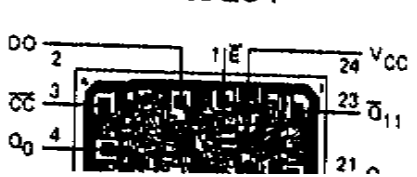
Metallization and Pad Layout

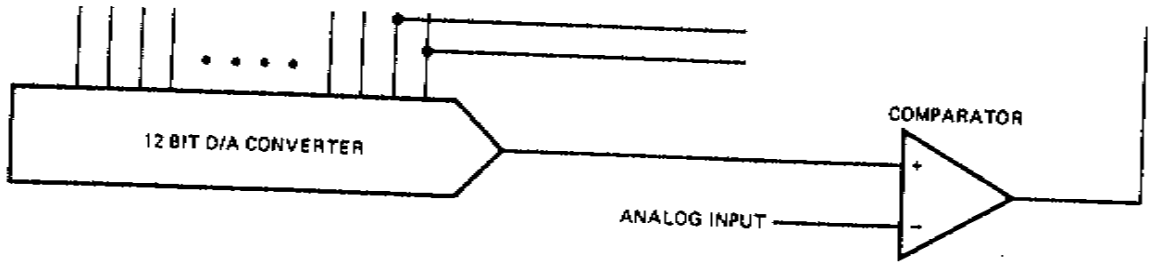
Am25L02

Am25L03



Am25L04





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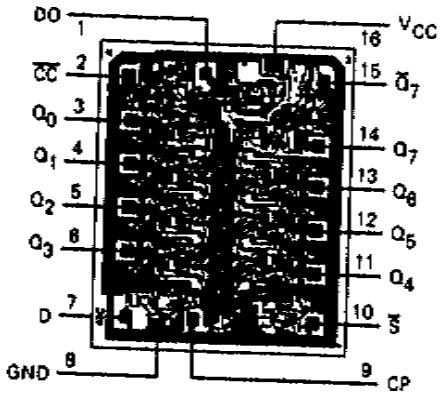
how the Am25L02/3/4 registers are used with a Digital-to-Analog converter and a comparator to form a very high-speed conversion Analog-to-Digital converter. Conversion time is limited mainly by the speed of the D/A converter and comparator conversion rates of 300,000 conversions per second. The comparator can be the Am111 precision comparator, or Am106 omparator.

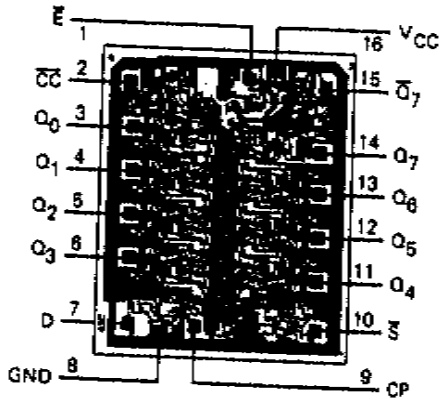
Metallization and Pad Layout

Am25L02



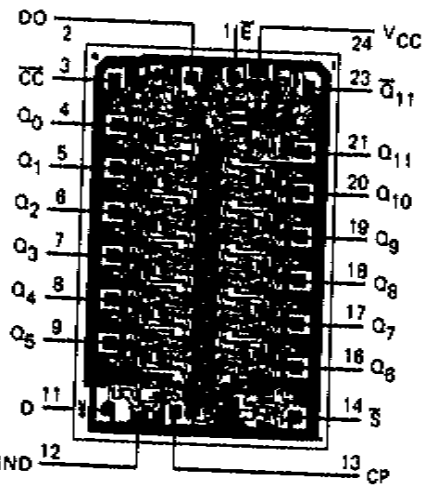
DIE SIZE 0.087" X 0.105"

Am25L03



DIE SIZE 0.087" X 0.105"

Am25L04



DIE SIZE 0.087" X 0.135"